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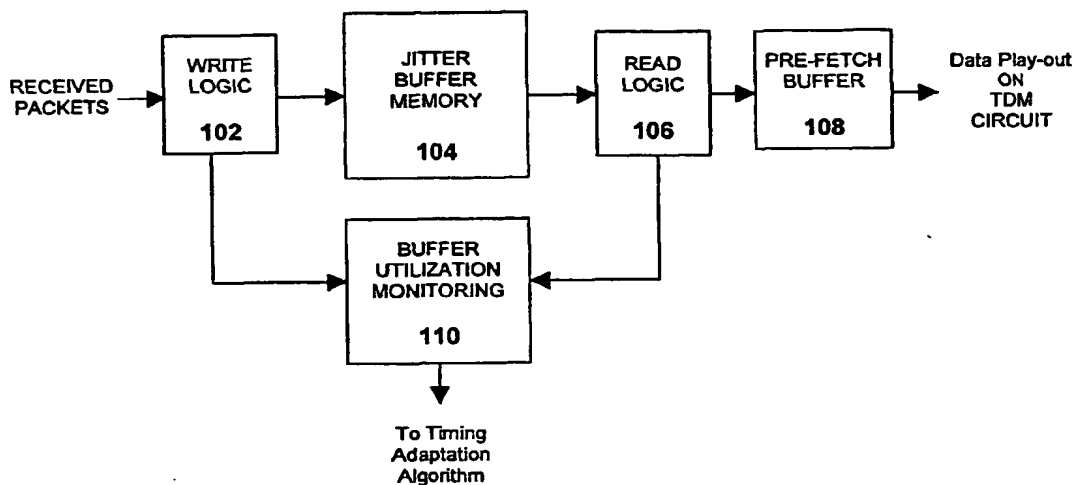
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(54) Title: METHOD AND APPARATUS FOR PARTITIONING ALLOCATION AND MANAGEMENT OF JITTER BUFFER  
MEMORY FOR TDM CIRCUIT EMULATION APPLICATIONS

**100**



(57) Abstract: A method for partitioning allocation and management of a jitter buffer memory for TDM circuit emulation applica-  
tions comprises the steps of obtaining a channel hierarchy for a plurality of packet carrying channels having different channel rates,  
obtaining a packet sequential number, and using the channel hierarchy and the packet sequential number, generating a base-address  
in the jitter buffer memory. Each channel is allocated a space in the buffer memory that is proportional to its rate, and out-of-order  
packets are automatically reordered by the jitter buffer.

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International application No.

PCT/IL04/00575

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H04J 3/06

US CL : 370/516

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/516,517,907;375/371,372

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 2003/0227943 A1 (HALLMAN ET AL) 11 December 2003 ( 11.12.2003), page 1, paragraph 0006-0007; page 4, paragraph 0054-0055; Figure 20.	1-19
A,P	US 6,665,317 B1 (SCOTT) 16 December 2003 (16.12.2003), column 2, lines 1-20.	1-19
A, P	US 2003/0219012 A1 ( WISLER et al) 27 November 2003 (27.11.2003), page 1, paragraph 0008.	1-19

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